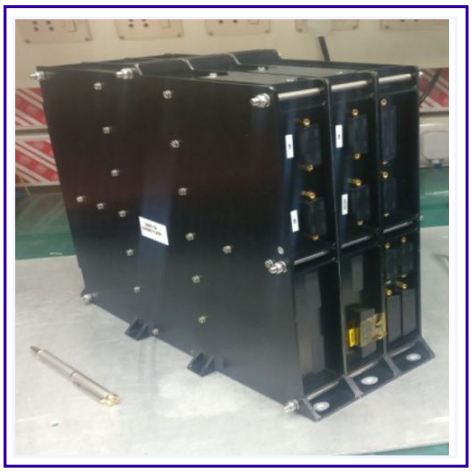
# Reprogrammable FPGA Based Data Handling System

U R Rao Satellite Centre (URSC) of Indian Space Research Organisation (ISRO) has developed Reprogrammable FPGA Based Data Handling System.

System is built around Xilinx Virtex 5 FPGA. Suitable for High data rate data handling system with Ser/Deser links for payload data interface.



## Salient Features

- Modular vertical mount package with mother board/ daughter board concept.
- System has capability to carry out on-board data processing.
- System is realized with active thermal control inside package.

## Major Specifications

- System design with programmable RHBD Xilinx Virtex-5 FPGA.
- Single Board capable of handling 9.76 Gbps throughput using high speed TLK2711 data link, CDCM clock cleaners, and Virtex-5 on chip memory and logic resources.
- 19Gbps System throughput, can be expandable by additional daughter boards.

## Technology Transfer

URSC/ISRO offers to transfer this technology of Reprogrammable FPGA Based Data Handling System developed by URSC to industries in India with adequate experience and facilities. Industries interested in obtaining knowhow may write giving details of their present activities, infrastructure and facilities.

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