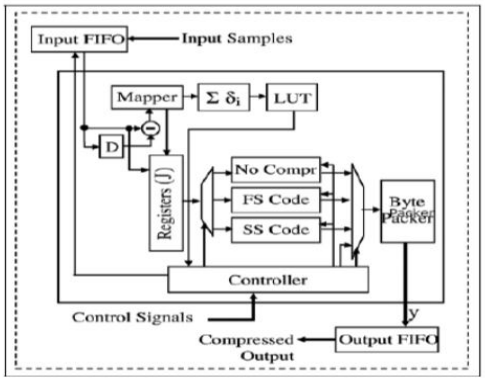
Rice Coder Compression System

U R Rao Satellite Centre (URSC) of Indian Space Research Organisation (ISRO) has developed CCSDS recommended Rice Coder.

The Rice Coder architecture is developed in accordance to CCSDS-121.0-B-1. Based on the pixel depth & hardware requirements, two different code option selection schemes are employed:

1. Optimum Method (As in CCSDS Document).
2. Heuristic Method for serial architecture. For parallel architecture only heuristic method is implemented to reduce the complexity.



RICE CODER

Salient Features

- Low complexity implementation.
- Hardware efficient Loss-less CCSDS Rice Coder.
- Configurable pixel depth.

Major Specifications

1	Pixel Depth	Configurable Bit depth (8 to 32 bit)	
2	Serial Architecture	Frequency of Operation(Max)	~ 35 MHz
		Input Pixel rate (Max)	~ 5 MSamples/sec
		Hardware resource utilization	~8 % cells (CC+RC) of RTAX2000 FPGA.
	High Speed Pipelined architecture	Frequency of Operation(Max)	~ 40 MHz
		Input Pixel rate (Max)	~ 26 MSamples/sec
		Hardware resource utilization	~ 9 % cells (CC+RC), 4 Memory Modules of RTAX2000 FPGA

Technology Transfer

URSC/ISRO offers to transfer this technology of CCSDS recommended Rice Coder developed by URSC to industries in India with adequate experience and facilities. Industries interested in obtaining knowhow may write giving details of their present activities, infrastructure and facilities.

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