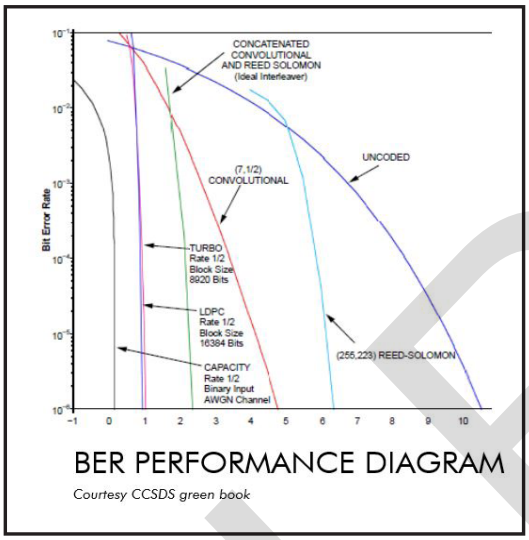
IP cores for Error control codes

U R Rao Satellite Centre (URSC) of Indian Space Research Organisation (ISRO) has developed IP cores for Error control codes.

Error control codes are mainly used to protect the transmitted data from channel errors and to provide coding gain. Various error control codes are implemented as part of Downlink chain of Data handling system. Type of the code chosen is dictated by various parameters like, link margin requirement, type of data to be transmitted, downlink profile and the amount of acceptable coding overhead etc.



BER PERFORMANCE DIAGRAM

Courtesy CCSDS green book

Salient Features

- Error control codes (ECC) developed in VHDL.
- ECC type could be selected as per the link requirements.
- Optimised for speed and area.
- CCSDS compatible.

Major Specifications

1.	RS Coders: RS(255,247), RS(255,239), RS(255,223),
2.	RS(255,239) + TCM(2/2.5/2.25/2.75,3)
3.	RS(255,223)+1/2 Convolutional coder
4.	LDPC
5.	Turbo codes with rate half

Technology Transfer

URSC-ISRO offers to transfer this technology IP cores for Error control codes developed by URSC to industries in India with adequate experience and facilities. Industries interested in obtaining knowhow may write giving details of their present activities, infrastructure and facilities.

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