

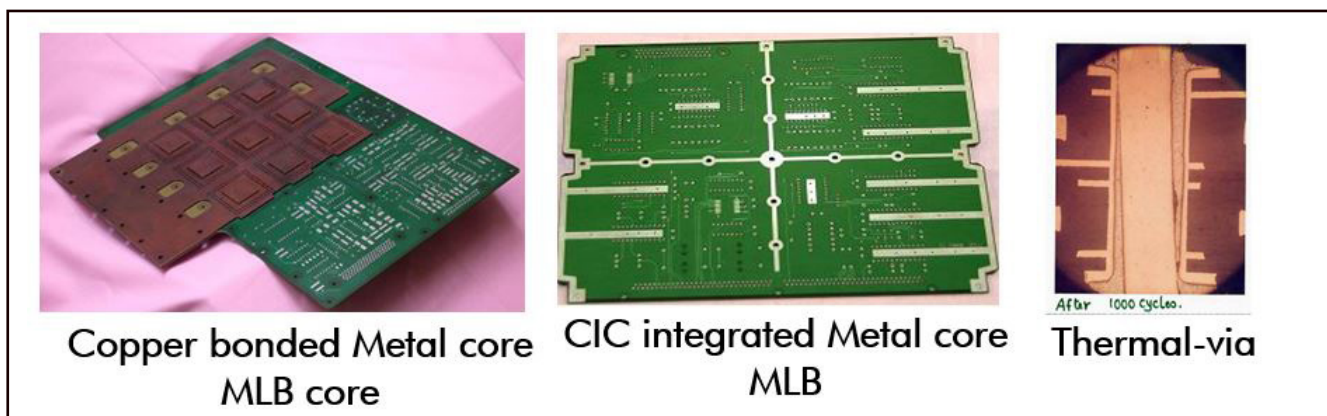
## Metal Core Multilayer PCB Technology for Thermal Management

U R Rao Satellite Centre (URSC) of Indian Space Research Organisation (ISRO) has developed Metal core multilayer PCB Technology for thermal management with

- Internally bonded Copper-Invar-Copper (CIC) and
- Externally bonded copper sheet onto PCB.

Metal core multilayer PCB with internally bonded CIC incorporating thermal vias are used for sinking the generated heat through distribution to the entire core area and then transferring the heat to the chassis connected with thermal vias.

Metal core multilayer PCB with externally bonded copper plate onto the finished PCB was used for controlling the temperatures of Detectors of payloads in Space Science Missions.



## Technology Transfer

URSC/ISRO offers to transfer this technology of Metal Core Multilayer PCB Technology for Thermal Management with internally bonded Copper-Invar-Copper (CIC) and externally bonded copper sheet onto PCB to industries in India with adequate experience and facilities. Industries interested in obtaining knowhow may write giving details of their present activities, infrastructure and facilities.

## Salient Features & Major specifications

Parameter	Specifications
Type of PCB	Metal core PCB with integrally bonded CIC, Metal core PCB with externally bonded copper
No. of layers	6 to 14 layers, as specified in layer stack diagram
Total PCB thickness	2.3 mm to 3.2 mm, as per the layer stack diagram
Metal core laminates (20:60:20)	6 mils thick (20:60:20) - CIC, complying with IPC-CF-152 specifications & Electronic grade copper plate of required thickness
Material for rigid laminate	Glass-epoxy, Tg > 175°C, complying to IPC 4101/24 or IPC 4101/29 specifications
Material for bonding inner layers	Glass-epoxy, Tg > 175°C, complying to IPC 4101/24 or IPC 4101/29 specifications
Clearance holes filling material in metal cores	Glass-epoxy prepreg with micro-dispersed ceramic filler system (for CIC), Tg > 175°C.
Prepregs for bonding	No-flow glass-polyimide (Cu bonding with PCB)
Dielectric separation	100 microns minimum
Inner layer copper thickness	70 microns (or 35 microns), as specified in the layer stack diagram
External layers copper thickness	70 microns to 105 microns, including 35 microns plated copper, as specified in ordering data sheet
Min. trace width / spacing	5 mils / 5 mils (125 microns)
Min. through hole dia.	0.40 mm, as specified in the ordering data sheet
Etchback	Positive etchback of 5 to 15 µm (preferred), complete desmear is also acceptable, negative etchback is not allowed.
Deposited Cu thickness	35 microns (± 10 microns)
Registration error	0.25 mm maximum, provided the requirement for minimum inner layer annular ring is met
Minimum conductor pad annular ring	50 microns - inner layers 130 microns - external layers
Multilayer Construction	Laminate type construction
Fabrication Technique	Subtractive process, Electroless Copper, SMOBC
Solder mask material	Electra EMP110 (or) Taiyo PSR-4000BN
Surface finish & specs	Eutectic Solder, Tin - 63% / Lead - 37%

Technology Transfer & Industry Coordination Division (TTID),  
Programme Planning and Evaluation Group (PPEG),

📍 U R Rao Satellite Centre (URSC), ISRO, HAL Airport Road,  
Vimanapura Post, Bangalore – 560 017.

✉ Email-id: tt-icd@ursc.gov.in

☎ Fax No: 080-25205261

🌐 <https://www.ursc.gov.in/industry/index.jsp>