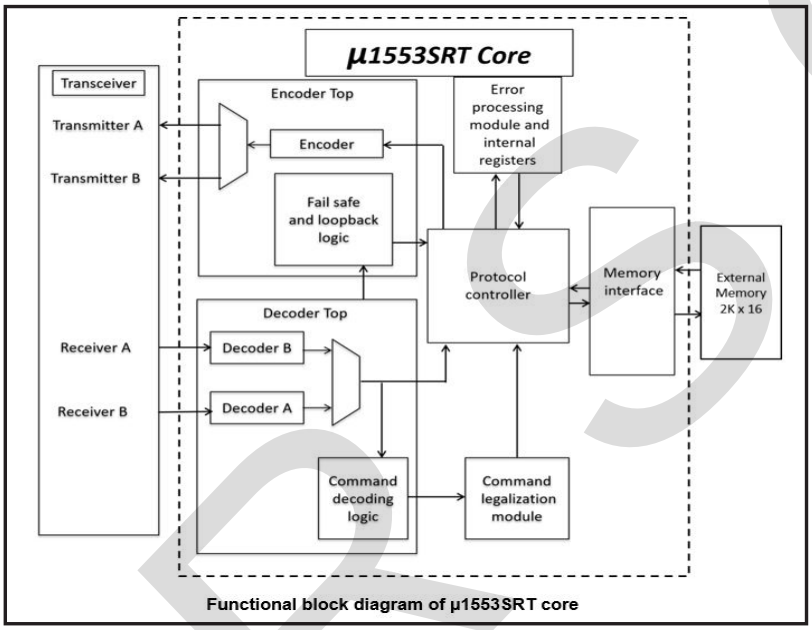
MIL-STD-1553B Simple Remote Terminal (μ1553SRT) IP core

U R Rao Satellite Centre (URSC) of Indian Space Research Organisation (ISRO) has developed a MIL-STD-1553B Simple Remote Terminal (μ1553SRT) IP Core as an IP core suitable for FPGA and ASIC designs. μ1553SRT IP core implements a dual redundant MIL-STD-1553B Notice II data bus Remote Terminal (RT).



Functional block diagram of μ1553SRT core

Salient Features

- Supports all MIL-STD-1553B transfer types, including RT-to-RT and broadcast transfers.
- Interfaces to standard 1553 transceivers.
- Selectable clock rate of 12 or 24 MHz.
- Supports 2K x 16 external memory.
- Synchronous or asynchronous memory interface.
- Fail safe Finite State Machines : Core resets itself in case it gets into faulty state.
- Fully synchronous operation with single clock domain.
- Continuous loop-back checking of transmitted MIL-STD-1553B data.

- Data wraparound feature for sub-address 30.
- Dedicated output that pulses on reception of a synchronize mode code.

Major Specifications

- Core compliant to specifications as per MIL-STD-1553B Notice II.
- Validation as per RT Validation Test Plan MIL-HDBK-1553, Appendix A.

Technology Transfer

URSC-ISRO offers to transfer this technology of MIL-STD-1553B Simple Remote Terminal (μ1553SRT) IP Core to industries in India with adequate experience and facilities. Industries interested in obtaining knowhow may write giving details of their present activities, infrastructure and facilities.

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