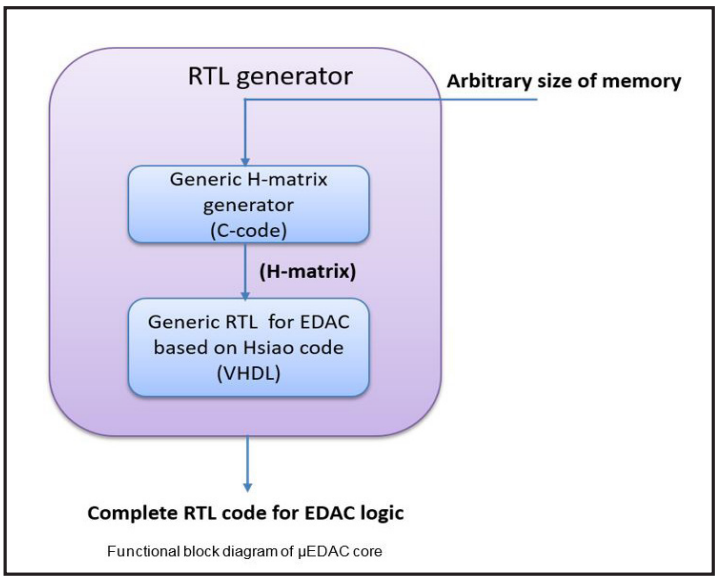
Generic EDAC (μEDAC) IP core

U R Rao Satellite Centre (URSC) of Indian Space Research Organisation (ISRO) has developed a Generic EDAC (μEDAC) IP Core which will generate Error Detection and Correction (EDAC) logic with Single Error Correction Double Error Detection (SEC-DED) capability, for user-specified memory size.

EDAC logic is widely used for protecting memories from Single Event Upsets (SEU), which occur in environments with high levels of radiation.



Functional block diagram of μEDAC core

Salient Features & Major specification

- Supports configurable memory size.
- Generates technology and vendor independent RTL code.
- EDAC encoder and decoder compatible with FPGA and ASIC designs.
- HSIAO code based EDAC for minimum circuit area and delay.
- EDAC check-matrix with minimum odd-weight non-equal columns and quasi-equal weight rows.
- Non-exponential order check-matrix generation which ensures quick RTL code generation even for large memory size.

Technology Transfer

URSC/ISRO offers to transfer this technology of Generic EDAC (μEDAC) IP Core to industries in India with adequate experience and facilities. Industries interested in obtaining knowhow may write giving details of their present activities, infrastructure and facilities.

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