Digital BPSK Demodulator and Bit Synchronizer ASIC

U R Rao Satellite Centre (URSC) of Indian Space Research Organisation (ISRO) has developed Digital BPSK Demodulator and Bit Synchronizer ASIC.

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Salient Features

- Programmable data rate and Carrier Frequency.
- Programmable Loop filter parameters for Demodulator and Bit synchronizer.
- Programmable Carrier Lock and Bit synchronizer Lock detector Threshold.
- On chip Programmable Sampling clock generation circuit.
- Implemented using efficient DSP algorithms for Filters and PLLs.
- Industry recommended highly efficient COSTAS Loop for Demodulator & In-Phase /Mid Phase Algorithm for Bit Synchronizer.
- Implementation loss of less than 1 dB.
- ASIC available in Rad hard 0.18 micron & 0.6-micron technology.

Major Specifications

Data rate	100 bps to 16 kbps
Carrier Frequency	900 Hz to 200 kHz
Carrier Acquisition time	Maximum 40 Bits
Bit synchronizer Acquisition Time	Maximum 120 bits
Sampling Frequency	7 kHz to 1.69 MHz
Input Level	4.5 ±0.5 Vpp(LF-155 Op-Amp input)
A/D Output	8 bits
Carrier Lock /Bit Sync Lock Indicator (Output)	0,1 (CMOS) 1 for Lock , 0 for Unlock
Power Consumption	Approx. 2 Watt for full system with Analog Front End
Eb/No Required for BER of $1X10^{-5}$	< 1 dB Loss

Technology Transfer

URSC/ISRO offers to transfer this technology of Digital BPSK Demodulator and Bit Synchronizer ASIC to industries in India with adequate experience and facilities. Industries interested in obtaining knowhow may write giving details of their present activities, infrastructure and facilities.

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